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CLEAN VERSION OF PENDING CLAIMS

HIGH OUTPUT HIGH EFFICIENCY LOW VOLTAGE CHARGE PUMP
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Claims 1-42, as of December 17, 2001 (Date of Response to Final Office Action and RCE).

1. (Twice Amended) A charge pump, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

2. (Twice Amended) A charge pump, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively,

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase

generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

3. A charge pump, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

4. The charge pump of claim 3, wherein the plurality of phase generators further comprises:

a primary phase generator;

a secondary phase generator coupled to the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator; and

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively.

5. A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator;

a secondary phase generator coupled to the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the primary phase generator during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the secondary phase generator during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

6. The charge pump of claim 5, further including a power source, wherein the power source includes an output voltage approximately in the range of about 1 to 2.5 volts.

7. The charge pump of claim 5, wherein the primary phase generator comprises:

an inverter, coupled to the oscillator to receive an input signal from the oscillator based on the phase cycle and providing output signals which are 180 degrees out of phase; and

cross coupled gates coupled to the inverter to receive the output signals from the inverter and outputting signals that are non-overlapping and crossing around high points of their signals during the first and second phases, respectively, and further outputting signals that are non-overlapping and crossing around low points of their signals during the first and second phases,

respectively.

8. The charge pump of claim 5, wherein the secondary phase generator comprising a delay circuit coupled to the primary phase generator, including an input receiving signals that are non-overlapping and crossing around high points of their signals from the primary phase generator, and providing an output signal similar to the input signal, and having a predetermined delay from the input signal.

9. The charge pump of claim 8, wherein the predetermined delay is approximately in the range of about 10 to 30 nanoseconds.

10. The charge pump of claim 8, wherein the first and second preboot capacitors coupled to the primary phase generator to receive input signals that are non-overlapping and crossing around high points and low points of their signals, and providing an output signal to preboot the first and second main capacitors to a first predetermined level during the first and second phases, respectively.

11. The charge pump of claim 10, wherein the first predetermined level is approximately in the range of about 1 to 5 volts.

12. The charge pump of claim 10, further comprising first and second precharge capacitors coupled to the primary phase generator and the first and second main pump capacitors, respectively, including an input receiving the signals that are non-overlapping and crossing around high points of their signals and providing an output signal to precharge the first and second main capacitors to a second predetermined level during the first and second phases, respectively.

13. The charge pump of claim 12, wherein the second predetermined level is approximately in the range of about 1 to 5 volts.

14. The charge pump of claim 12, wherein the first and second precharge capacitors further comprising transistors to precharge the first and second precharge capacitors.

15. The charge pump of claim 14, wherein the first and second main pump capacitors coupled to the secondary phase generator, and the first and second precharge capacitors, respectively, including an input receiving the delayed signal from the secondary phase generator to move the second predetermined level to a third predetermined level, and dumping an output during the first and second phases, respectively.

16. The charge pump of claim 15, wherein the third predetermined level is approximately in the range of about 1 to 5 volts.

17. The charge pump of claim 15, wherein the first and second gating devices coupled to the first and second main pump capacitors, including an input receiving the dumped signal from the first and second main pump capacitors and an output outputting a charge to an external load.

18. The charge pump of claim 15, wherein the outputting charge is approximately in range of about 1.5 to 5 volts.

19. A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator;

a secondary phase generator coupled to the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator;

first and second main pump capacitors coupled to the secondary phase generator, and the

first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level of approximately in the range of about 1 to 5 volts by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level of approximately in the range of about 1 to 5 volts in response to the primary phase generator during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level of approximately in the range of about 1 to 1.5 volts in response to the secondary phase generator during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

20. A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator further includes;

an inverter, coupled to the oscillator to receive an input signal from the oscillator based on the phase cycle and providing output signals which are 180 degrees out of phase; and

cross coupled gates coupled to the inverter to receive the output signals from the inverter and outputting signals that are non-overlapping and crossing around high points of their signals during the first and second phases, respectively, and further outputting signals that are non-overlapping and crossing around low points of their signals during the first and second phases, respectively;

a secondary phase generator coupled to the primary phase generator receives the signals that are non-overlapping and crossing around high points of their signals from the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator receives the

signals that non-overlapping and crossing around high points and low points of their signals from the primary phase generator;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the primary phase generator during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the secondary phase generator during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

21. A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

first and second primary phase generators coupled to the oscillator;

first and second secondary phase generators coupled to the first and second primary phase generators, respectively;

first and second preboot capacitors coupled to the first and second primary phase generators, respectively;

a first main pump capacitor coupled to the first secondary phase generator, and the first preboot capacitor;

a second main pump capacitor coupled to the second secondary phase generator, and the second preboot capacitor;

a first and second p-channel gates coupled to the first and second main pump capacitors, respectively;

wherein the first main pump capacitor is prebooted to a first pre-determined level by the second preboot capacitor during the first phase, wherein the first pre-determined level moves to a second pre-determined level during the second phase in response to the first primary phase generator, wherein the second predetermined level moves to a third predetermined level in response to the first secondary phase generator, and wherein the third predetermined level dumped to a first p-channel gate during the first phase; and

wherein the second main pump capacitor is prebooted to a first pre-determined level by the first preboot capacitor during the second phase, wherein the first predetermined level moves to a second pre-determined level during the first phase in response to the second primary phase generator, wherein the second predetermined level moves to a third predetermined level in response to the second secondary phase generator, and wherein the third predetermined level dumped to a second p-channel gate during the second phase.

22. A charge pump circuit, comprising:

a phase generator to generate a first and a second phase during a phase cycle;

a primary phase generator, coupled to the phase generator, wherein the primary phase generator includes a first and a second phase generator to generate a first and a second phase signal that are non-overlapping and crossing each other substantially around their high points during the phase cycle, wherein the primary phase generator further generates a third and a fourth phase signal that are non-overlapping and crossing around their low points during the phase cycle, and wherein the primary phase generator further generates a seventh and a eighth phase signal;

a secondary phase generator, coupled to the primary phase generator, wherein the secondary phase generator includes a first and a second secondary phase generator to generate a fifth and sixth phase signal similar to first and second phase signal, and including a predetermined delay from the first and second phase signal;

a first and a second main energy storing device;

a first and a second pre-boosting stage, coupled to the first and second primary phase

generators respectively, wherein the first and second pre-boosting stages boosts the first and second main energy storing devices to a first predetermined boost level during the first and second phases respectively; and

a first and a second pre-charging stage, coupled to the first and second main energy storing devices, wherein the first and second pre-charging stages further boost the first and second main energy storing devices to a second predetermined boost level during the first and second phases respectively, wherein the first and second main energy storing devices are further boosted to a third predetermined boost level by the fifth and sixth phase signals to allow the first and second main energy storing devices to output a desired level of a high-voltage signal during the first and second phases.

23. A two-phase integrated circuit charge pump, comprising:

an oscillator, where the oscillator generates an oscillating signal during a phase cycle including a first and a second phase;

a primary phase generator, coupled to the oscillator, wherein the primary phase generator generates a first phase signal and a second phase signal that are non-overlapping and crossing each other around high points of their signals during a phase cycle, further the primary phase generator generates a third phase signal and a fourth phase signal that are non-overlapping and crossing each other around low points of their signals during every phase cycle, and further the primary phase generator generates a seventh phase signal and an eighth phase signal;

a secondary phase generator, coupled to the primary phase generator, wherein the secondary phase generator receives the first and second phase signals and generates a fifth phase signal and a sixth phase signal that are non-overlapping and crossing each other around high points of their signals during a phase cycle and includes a predetermined delay from the first and second phase signals;

a first and second pre-boot precharge capacitors, coupled to the primary phase generator, wherein the first and second pre-boot precharge capacitors receive the third and fourth phase signals from the primary phase generator during the first and second phases respectively;

a first and second pre-boot capacitors, coupled to the primary phase generator and the first and second pre-boot precharge capacitors respectively, receives the first and second phase signals from the primary phase generator respectively, and wherein the first and second pre-boot precharge capacitors pre-charges the first and second pre-boot capacitors to a pre-determined level during the first and second phases respectively;

a first and second main pump precharge capacitors, coupled to the primary phase generator, wherein the first and second main pump precharge capacitors receive the seventh and eighth phase signals from the primary phase generator during the first and second phases respectively;

a first main pump capacitor, coupled to the first main pump precharge capacitor, the second pre-boot capacitor, and the secondary phase generator, wherein the second pre-boot capacitor pre-boots the first main pump to a predetermined booted level during the first phase, further the first main pump precharge capacitor precharges the first main pump capacitor to a second pre-determined level during the second phase and further the first main pump capacitor receives the fifth phase signal from the secondary phase generator during the first phase, and where the first main pump capacitor goes to a third predetermined level and outputs a charge to a first p-channel gate during the first phase; and

a second main pump capacitor, coupled to the second main pump precharge capacitor, the first pre-boot capacitor, and the secondary phase generator, wherein the first pre-boot capacitor pre-boots the second main pump to a predetermined booted level during the second phase, further the second main pump precharge capacitor precharges the second main pump capacitor to a second pre-determined level during the first phase, and further the second main pump capacitor receives the sixth phase signal from the secondary phase generator during the second phase, and where the second main pump capacitor goes to the third predetermined level and outputs the charge to a second p-channel gate during the second phase.

24. A two-phase charge pump for producing a pump voltage on an output line, comprising:

an oscillator, where the oscillator generates an oscillating signal;

a primary phase generator, coupled to the oscillator, generates a first phase signal and a second phase signal that are non-overlapping and crossing each other around high points of their signals during every phase cycle (consisting of a first phase and a second phase), further the primary phase generator generates a third phase signal and a fourth phase signal that are non-overlapping and crossing each other around low points of their signals during every phase cycle, and further the primary phase generator generates a seventh phase signal and a eighth phase signal;

a delay element, coupled to the primary phase generator, receives the first and second phase signals and generates a fifth phase signal and a sixth phase signal that are non-overlapping and crossing each other around high points of their signals during every phase cycle and includes a predetermined delay from the first and second phase signals;

a first and second pre-boot precharge circuitry, coupled to the primary phase generator, receives the third and fourth signals from the primary phase generator during a first and second phases respectively;

a first and second pre-boot circuitry, coupled to the primary phase generator and the first and second pre-boot precharge capacitors respectively, receives the first and second phase signals from the primary phase generator respectively, and where the first and second pre-boot precharge circuitry pre-charges the first and second pre-boot capacitors to a pre-determined level during the first and second phases respectively;

a first and second main pump precharge circuitry, coupled to the primary phase generator receives the seventh and eighth phase signals from the delay element during the first and second phases respectively;

a first main pump circuitry, coupled to the first main pump precharge circuitry, the second pre-boot circuitry, and the delay element, where the second pre-boot circuitry pre-boots the first main pump circuitry to a predetermined booted level during the first phase, further the first main pump precharge circuitry precharges the first main pump circuitry to a second pre-determined level during the second phase and further the first main pump circuitry receives the fifth phase signal from the delay element during the first phase, and where the first main pump

circuitry goes to a third predetermined level and outputs a charge to a first p-channel gate during the first phase; and

a second main pump circuitry, coupled to the second main pump precharge circuitry, the first pre-boot circuitry, and the delay element, where the first pre-boot circuitry pre-boots the second main pump to a predetermined booted level during the second phase, further the second main pump precharge circuitry precharges the second main pump circuitry to a second pre-determined level during the first phase, and further the second main pump circuitry receives the sixth phase signal from the delay element during the second phase, and where the second main pump circuitry goes to the third predetermined level and outputs the charge to a second p-channel gate during the second phase.

25. A charge pump circuit, comprising:

a phase generator to generate a first phase and a second phase, wherein the first phase is 180 degrees out of phase with respect to the second phase;

a primary phase generator, coupled to the oscillator, generates a first phase signal and a second phase signal that are non-overlapping and crossing each other around high points of their signals during every phase cycle (consisting of a first phase and a second phase), further the primary phase generator generates a third phase signal and a fourth phase signal that are non-overlapping and crossing each other around low points of their signals during every phase cycle, and further the primary phase generator generates a seventh phase signal and a eighth phase signal;

a secondary phase generator, coupled to the primary phase generator, receives the first and second phase signals and generates a fifth phase signal and a sixth phase signal that are non-overlapping and crossing each other around high points of their signals during every phase cycle and includes a predetermined delay from the first and second phase signals;

a first and second pre-boot precharge capacitors, coupled to the primary phase generator, receives the third and fourth signals from the primary phase generator during a first and second phases respectively;

a first and second pre-boot capacitors, coupled to the primary phase generator and the first and second pre-boot precharge capacitors respectively, receives the first and second phase signals from the primary phase generator respectively, and where the first and second pre-boot precharge capacitors pre-charges the first and second pre-boot capacitors to a pre-determined level during the first and second phases respectively;

a first and second main pump precharge capacitors, coupled to the primary phase generator receives the seventh and eighth phase signals from the primary phase generator during the first and second phases respectively;

a first main pump capacitor, coupled to the first main pump precharge capacitor, the second pre-boot capacitor, and the secondary phase generator, where the second pre-boot capacitor pre-boots the first main pump to a predetermined booted level during the first phase, further the first main pump precharge capacitor precharges the first main pump capacitor to a second pre-determined level during the second phase and further the first main pump capacitor receives the fifth phase signal from the secondary phase generator during the first phase, and where the first main pump capacitor goes to a third predetermined level and outputs a charge to a first p-channel gate during the first phase; and

a second main pump capacitor, coupled to the second main pump precharge capacitor, the first pre-boot capacitor, and the secondary phase generator, where the first pre-boot capacitor pre-boots the second main pump to a predetermined booted level during the second phase, further the second main pump precharge capacitor precharges the second main pump capacitor to a second pre-determined level during the first phase, and further the second main pump capacitor receives the sixth phase signal from the secondary phase generator during the second phase, and where the second main pump capacitor goes to the third predetermined level and outputs the charge to a second p-channel gate during the second phase.

26. (Twice Amended) A memory device, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

27. A memory device, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

28. (Twice Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

29. (Twice Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

30. A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase

generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

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31. (Twice Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

32. A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

33. (Twice Amended) An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase

generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled to the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

34. An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and second gating devices, during the first and second phases, respectively.

35. A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

recharging a pre-boot capacitor to a first pre-determined level during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level during a second phase;

pre-charging a first main pump capacitor to a second pre-determined level during the second phase;

boosting the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a V_{ccp} during the first phase;

pre-charging the second main pump capacitor to the second pre-determined level during the first phase;

boosting the second main pump to the third pre-determined level during the second phase; and

outputting the second main pump charge to a V_{ccp} during the second phase.

36. A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

recharging a pre-boot capacitor to a first pre-determined level during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level during a second phase;

pre-charging a first main pump capacitor to a second pre-determined level during the second phase;

boosting the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

pre-charging the second main pump capacitor to the second pre-determined level during the first phase;

boosting the second main pump to the third pre-determined level during the second phase; and

outputting the second main pump charge to a second p-channel gate during the second phase.

37. A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

recharging a pre-boot capacitor to a first pre-determined level during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level during a second phase;

pre-charging a first main pump capacitor to a second pre-determined level during the second phase;

boosting the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

outputting the charge from the first p-channel gate to a V_{ccp};

pre-charging the second main pump capacitor to the second pre-determined level during the first phase;

boosting the second main pump to the third pre-determined level during the second phase;

outputting the second main pump charge to a second p-channel gate during the second phase; and

outputting the charge from the second p-channel gate to a V_{ccp}.

38. A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

generating signals that are non-overlapping and crossing each other around high points of their signals;

generating signals that are non-overlapping and crossing each other around low points of their signals;

generating signals having a predetermined delay from the signals that are non-overlapping and crossing each other around high points;

recharging a first pre-boot capacitor to a first pre-determined level using the signals that are non-overlapping and crossing around the high points of their signals during a first phase;

recharging a second pre-boot capacitor to the first pre-determined level using the signals that are non-overlapping and crossing around the low points of their signals during a second phase;

pre-charging the first main pump capacitor to a second pre-determined level by the signals that are non-overlapping and crossing around the low points of their signals during the second phase;

inputting the signals having a predetermined delay to boost the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

outputting the charge from the first p-channel gate to a V_{ccp};

pre-charging the second main pump capacitor to the second pre-determined level by the signals that are non-overlapping and crossing around the low points of their signals during the first phase;

inputting the signals having a predetermined delay to boost the second main pump to the third pre-determined level during the second phase;

outputting the second main pump charge to a second p-channel gate during the second phase; and

outputting the charge from the second p-channel gate to a V_{ccp}.

39. A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

generating an oscillating signal;

generating a first and second phase signals that are non-overlapping and crossing each other around high points of their signals during every phase cycle from the oscillating signal by a primary phase generator;

generating a third and fourth phase signals that are non-overlapping and crossing each other around low points of their signals during every phase cycle from the oscillating signal by the primary phase generator;

generating a fifth and sixth phase signals having a predetermined delay from the first and second phase signals that are non-overlapping and crossing each other around high points from the first and second phase signals received from the primary phase generator by a secondary phase generator;

generating a seventh and eighth phase signals by the primary phase generator;

recharging a first pre-boot capacitor to a first pre-determined level using the first and third phase signals during the first phase;

recharging a second pre-boot capacitor to the first pre-determined level using the second and fourth phase signals during the second phase;

pre-booting a first main pump capacitor to the pre-determined boot level by the second pre-boot capacitor during the first phase;

pre-booting a second main pump capacitor to a pre-determined boot level by the first pre-boot capacitor during the second phase;

pre-charging the first main pump capacitor to a second pre-determined level by the seventh phase signal during the second phase;

inputting the fifth phase signal to boost the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

outputting the charge from the first p-channel gate to a V_{ccp};

pre-charging the second main pump capacitor to the second pre-determined level by the eight phase signal during the first phase;

inputting the sixth phase signal to boost the second main pump to the third pre-determined level during the second phase;

outputting the second main pump charge to a second p-channel gate during the second phase; and

outputting the charge from the second p-channel gate to a V_{ccp}.

40. A method of producing a pump supply voltage from an integrated circuit two phase charge pump, comprising:

generating an oscillating signal;

generating a first and second phase signals that are non-overlapping and crossing each other around high points of their signals during every phase cycle from the oscillating signal by a primary phase generator;

generating a third and fourth phase signals that are non-overlapping and crossing each other around low points of their signals during every phase cycle from the oscillating signal by the primary phase generator;

generating a fifth and sixth phase signals having a predetermined delay of approximately in the range of about 10 to 30 nanoseconds from the first and second phase signals that are non-overlapping and crossing each other around high points from the first and second phase signals received from the primary phase generator by a secondary phase generator;

generating a seventh and eighth phase signals by the primary phase generator;

recharging a first pre-boot capacitor to a first pre-determined level of approximately in the range of about 1 to 5 volts using the first and third phase signals during the first phase;

recharging a second pre-boot capacitor to the first pre-determined level of approximately in the range of about 1 to 5 volts using the second and fourth phase signals during the second phase;

pre-booting a first main pump capacitor to the pre-determined boot level of approximately in the range of about 1 to 5 volts by the second pre-boot capacitor during the first phase;

pre-booting a second main pump capacitor to a pre-determined boot level of approximately in the range of about 1 to 5 volts by the first pre-boot capacitor during the second phase;

pre-charging the first main pump capacitor to a second pre-determined level of approximately in the range of about 1 to 5 volts by the seventh phase signal during the second phase;

inputting the fifth phase signal to boost the first main pump to a third pre-determined level of approximately in the range of about 1 to 5 volts during the first phase;

outputting the first main pump charge to a first p-channel gate during the first phase;

outputting the charge from the first p-channel gate to a V_{ccp};

pre-charging the second main pump capacitor to the second pre-determined level approximately in the range of about 1 to 5 volts by the eight phase signal during the first phase;

inputting the sixth phase signal to boost the second main pump to the third pre-determined level of approximately in the range of about 1 to 5 volts during the second phase;

outputting the second main pump charge to a second p-channel gate during the second phase; and

outputting the charge from the second p-channel gate to a V_{ccp}.

41. A method of producing a pump supply voltage in an integrated circuit, the method, comprising:

generating an oscillating signal;

generating a first and second phase signals that are non-overlapping and crossing each other around high points of their signals during every phase cycle from the oscillating signal by a primary phase generator;

generating a third and fourth phase signals that are non-overlapping and crossing each other around low points of their signals during every phase cycle from the oscillating signal by the primary phase generator;

generating a fifth and sixth phase signals from the first and second phase signals, where the fifth and sixth phase signals are similar to the first and second phase signals, and having a predetermined delay from the first and second phase signals by a secondary phase generator;

generating a seventh and eighth phase signals by the primary phase generator;

recharging a first pre-boot capacitor to a first pre-determined level using the first and third phase signals during the first phase;

recharging a second pre-boot capacitor to the first pre-determined level using the second

and fourth phase signals during the second phase;

pre-booting a first main pump capacitor to the pre-determined boot level by the second pre-boot capacitor during the first phase;

pre-booting a second main pump capacitor to a pre-determined boot level by the first pre-boot capacitor during the second phase;

recharging the first main pump capacitor to a second pre-determined level by the seventh phase signal during the second phase;

inputting the fifth phase signal to raise the first main pump to a third pre-determined level during the first phase;

outputting the first main pump charge to a V_{ccp} during the first phase;

pre-charging the second main pump capacitor to the second pre-determined level by the eight phase signal during the first phase;

inputting the sixth phase signal to raise the second main pump to the third pre-determined level during the second phase; and

outputting the second main pump charge to the V_{ccp} during the second phase.

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42. (New) The charge pump of claim1, further comprising:

first and second sharing transistors coupled to the first and second pre-boot pre-charge capacitors and the first and second pre-boot capacitors to provide a path that charge shares the first and second pre-boot capacitors to the first and second main pump capacitors.